This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-52. (Cancelled)

53. (previously presented) A method for determining when to perform an error recovery instruction, comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface for an idle condition;

withholding access to a local processor and performing the error recovery instruction in response to detecting an idle condition in said processor interface before expiration of said timeout task, wherein the withholding access to a local processor further comprises withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating data transfer paths in the processor interface to determine when the data paths are idle, wherein the instruction performing while access to the local processor is withheld includes performing the error recovery instruction when the data transfer paths are idle;

forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires; and

resuming normal operations after performing the error recovery instruction.

54-63. (Cancelled)

64. (new) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform operations for determining when to perform an error recovery instruction, the operations comprising:

receiving an error recovery instruction;

beginning a timeout task;

monitoring a processor interface for an idle condition;

withholding access to a local processor and performing the error recovery instruction in response to detecting an idle condition in said processor interface before expiration of said timeout task, wherein the withholding access to a local processor further comprises withholding access to the processor interface when the idle condition is detected;

after access to the processor interface is withheld, interrogating data transfer paths in the processor interface to determine when the data paths are idle, wherein the instruction performing while access to the local processor is withheld includes performing the error recovery instruction when the data transfer paths are idle;

forcing performance of the error recovery instruction before an idle condition in said processor interface is detected when the timeout task expires; and

resuming normal operations after performing the error recovery instruction.

65. (new) An apparatus for use with a local processor and for quiescing processor control logic upon receipt of an error recovery instruction, comprising:

self-quiesce logic for receiving an error recovery instruction; and

a timer, coupled to the self-quiesce logic, for determining when to force execution of the error recovery instruction;

wherein the self-quiesce logic is adapted to begin a timeout task and initiate the timer when the error recovery instruction is received, begin to monitor a processor interface for an idle condition, detect an idle condition in said processor interface before expiration of said timer; in response to said detection, withhold access to a local processor, perform the error recovery instruction while access to the local processor is withheld, and force performance of the error recovery instruction before an idle condition in said processor interface is detected when the timer expires wherein after access to the processor interface is withheld, interrogate data transfer paths in the processor interface to determine when the data paths are idle, wherein the instruction performing while access to the local processor is withheld includes performing the error recovery instruction when the data transfer paths are idle, and resume normal operations after performing the error recovery instruction.